

EISCAT_3D
Active element subsystem
design document

Gudmund Wannberg and Ingemar Wolf

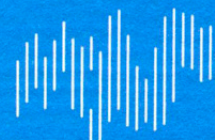
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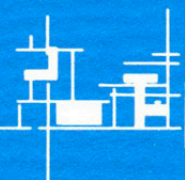
INSTITUTET FÖR RYMDFYSIK

Swedish Institute of Space Physics

Kiruna, Sweden



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EISCAT_3D DELIVERABLE 6.2: ACTIVE ELEMENT SUBSYSTEM DESIGN

Gudmund Wannberg and Ingemar Wolf
Swedish Institute of Space Physics
Box 812
SE-98128 Kiruna, Sweden
ugw@irf.se, ingemar.wolf@irf.se

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Preface

This Deliverable reports results from Work Package 6, “Active Element Subsystem Design”.

Noting that there would be at least a three-year delay from the completion of the present FP6-sponsored feasibility study to the actual placing of orders for a full-size EISCAT_3D system, and that major – largely unpredictable – changes in the RF semiconductor market situation can be expected during this time, the WP6 team decided at an early stage that no attempt should be made to produce a complete blueprint for a RF/antenna unit under the present contract.

Our efforts have instead focussed on resolving issues of a fundamental nature, where the results and conclusions will have a direct bearing on the detailed design work that must follow once the community has committed to the construction of the new radar system, irrespective of the design approaches taken at the component level.

The present Deliverable is essentially a compilation of three separate reports, covering three important areas of the Active Subsystem, i.e. the elementary transceiver/antenna combination to be used as the basic building block in the construction of the EISCAT_3D Core array.

The three reports address:

- The transmitter power amplifier,
- The transmit-receive switch, and
- The element antennas.

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EISCAT_3D WP6 TECHNICAL NOTE

ACTIVE ELEMENT POWER AMPLIFIERS

TESTS AND RESULTS

Gudmund Wannberg and Ingemar Wolf
Swedish Institute of Space Physics
Box 812
SE-98128 Kiruna, Sweden
ugw@irf.se

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Introduction

A detailed description of the EI_3D power device test bed and the test programme planned for it is given in Deliverable 6.1 “Interim Report” and will not be repeated here.

At the time of publication of D 6.1, the test bed had been fully configured, preliminary test runs had been completed and the following items remained to be addressed:

- A 1000-hour thermal-stress operation was to be started around February 10,
- Thereafter, a series of short-pulse (1- μ s), high-rep-rate (2 kHz) tests would be run,
- A multicarrier (OFDM) driving signals would be used to investigate the instantaneous power bandwidth and linearity of the amplifier chain,
- The amplifier noise floor in the powered-up OFF state would be measured,
- Detailed phase noise tests would be run on each individual amplifier and on the complete amplifier chain, both when powered from switch-mode PSUs and when powered from storage batteries,
- Tests at reduced drain voltage and reduced drive would be carried out to determine how well the amplifiers lend themselves to operating in a low-power mode.

Several of these have now been addressed and the results are reported below.

The “1000-hour” high-power test run

During the time period February 6 – March 11, 2009, an extended high-power test of the two second-generation (heat-spreader-equipped) BLF248 power amplifiers was carried out.

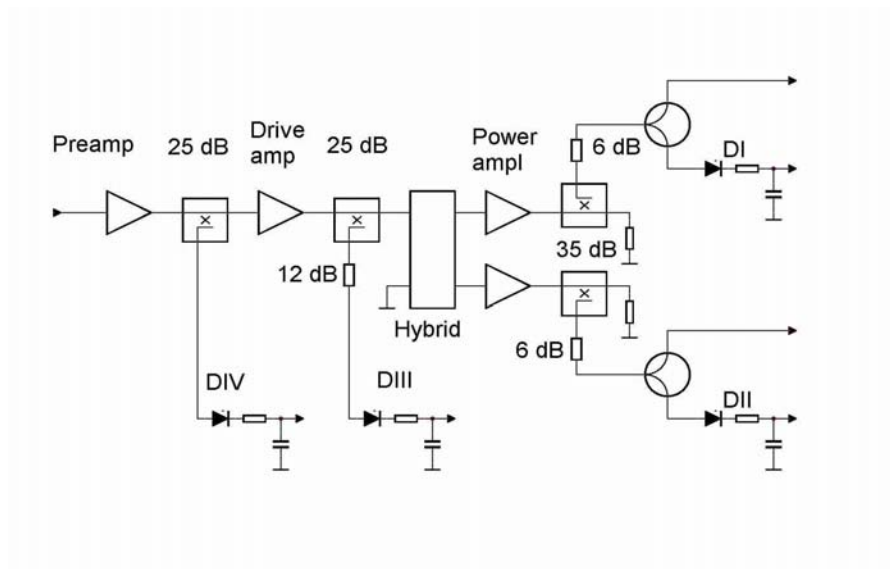


Figure 1: Simplified schematic diagram of the RF power test bed. Directional couplers for power measurements are labelled with their respective coupling coefficients in dB.

The initial plan was to run the amplifiers continuously at the 250-watt level for at least 1000 hours, but the run had to be terminated after 792 hours of continuous operation due to a power break for line maintenance requested by the local utility company.

For these tests, the amplifiers were excited with a waveform exposing the active devices to the worst possible thermal stress conditions that the amplifiers are expected to be subject to in actual radar operation. This waveform consists of a 2-millisecond pulse of un-modulated 235-MHz carrier, followed by a 6-millisecond OFF period, during which all gate biases are switched off, thus effectively interrupting the drain currents in all active devices and allowing them to cool down before the next pulse.

Temperature and RF power data

A data logger connected to the test bed was set up to record seven different parameters:

- Ambient temperature,
- Final amplifier #1 heatsink temperature,
- Final amplifier #2 heatsink temperature,
- Preamplifier RF output power,
- Driver amplifier RF output power,
- Final amplifier #1 RF output power,
- Final amplifier #2 RF output power.

Two calibrated Pt100 sensors, inserted into narrow holes drilled into the heatsinks from the side, approx. 1 mm below the heatsink surfaces, enabled the monitoring of temperature variations immediately underneath the respective BLF248 transistors. The RF power samples from the directional couplers were rectified by diode detectors, individually calibrated with 25% duty factor pulsed RF to replicate the test conditions as closely as possible; the diode output voltages were then smoothed by RC networks with a time constant of 0.1 s.

Parameter values logged during the time interval February 13 – March 11, 2009 are shown below. In each Figure, the data are organised as follows:

Upper panel:	Red -	ambient temperature [°C]
	Blue -	heatsink temperature, power amplifier 1 [°C]
	Green -	heatsink temperature, power amplifier 2 [°C]
Centre panel:	Blue -	output power, power amplifier 1 [dBm]
	Green -	output power, power amplifier 2 [dBm]
Lower panel:	Blue -	driver amplifier output power,
	Green -	preamplifier output power + 12.5 [dBm]

All parameters except the temperatures are displayed at the full sampling resolution, 10 s/sample. The temperature data are smoothed with a 5-minute running mean. The preamplifier output power values have a constant of 12.5 dB added to them in order to make it possible to plot them in the same expanded scale as the driving amplifier power values; the actual preamplifier output power level is thus obtained by subtracting 12.5 dB from the displayed values and is in the order of 31 dBm.

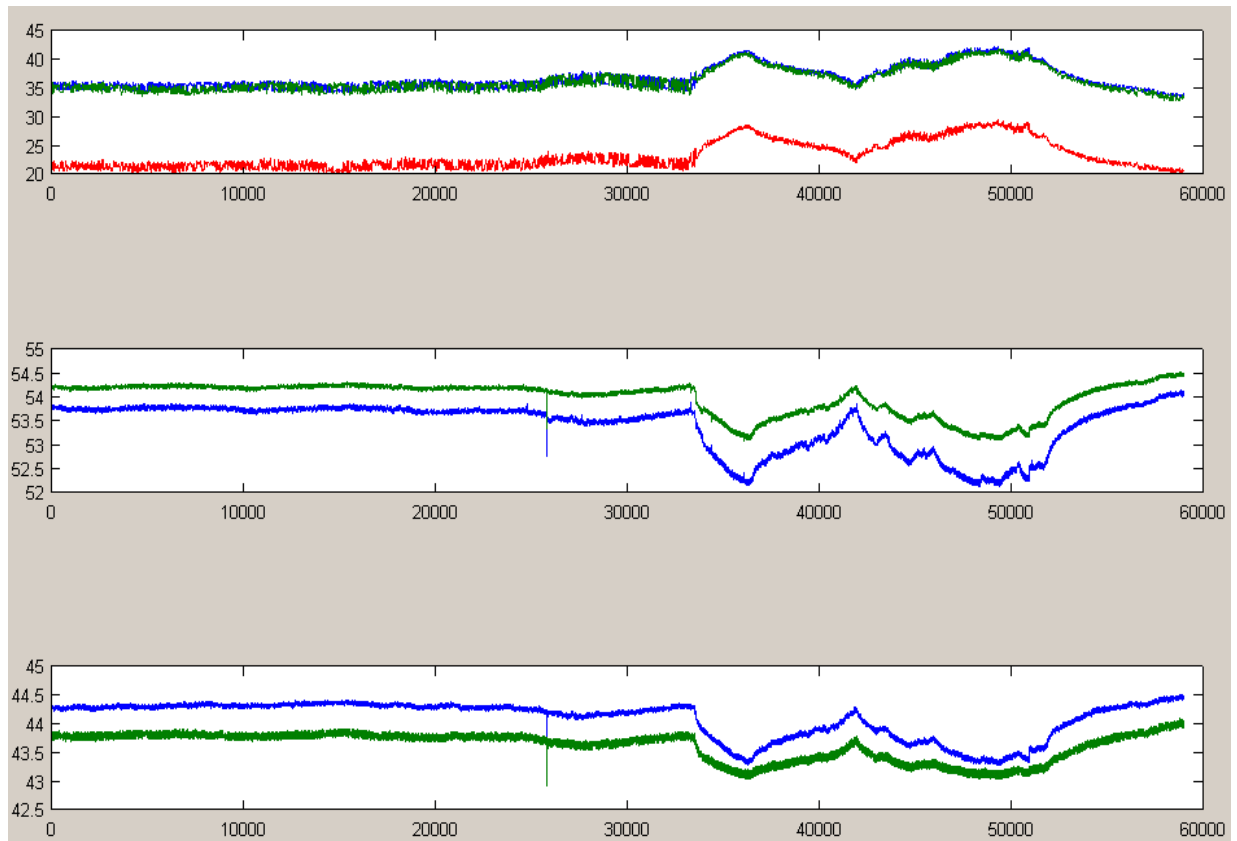


Figure 2: Data from February 13-19, 2009

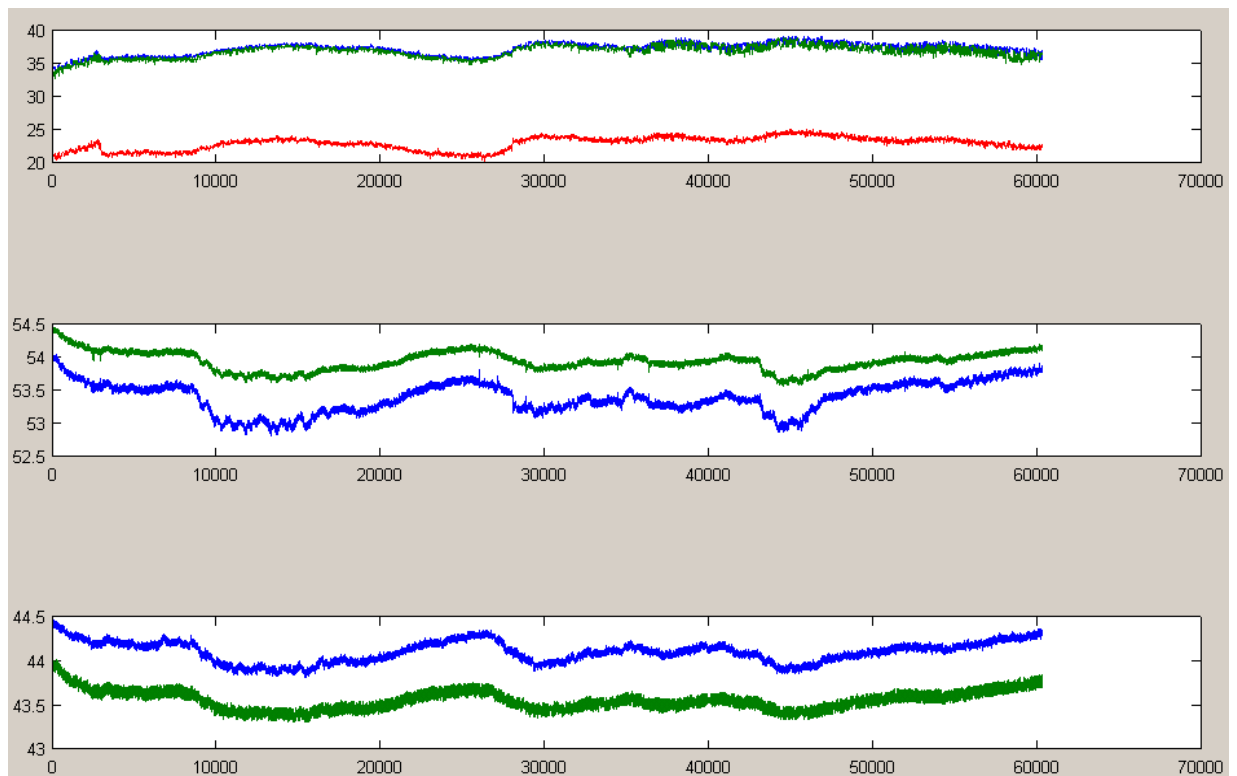


Figure 3: Data from February 20-27, 2009

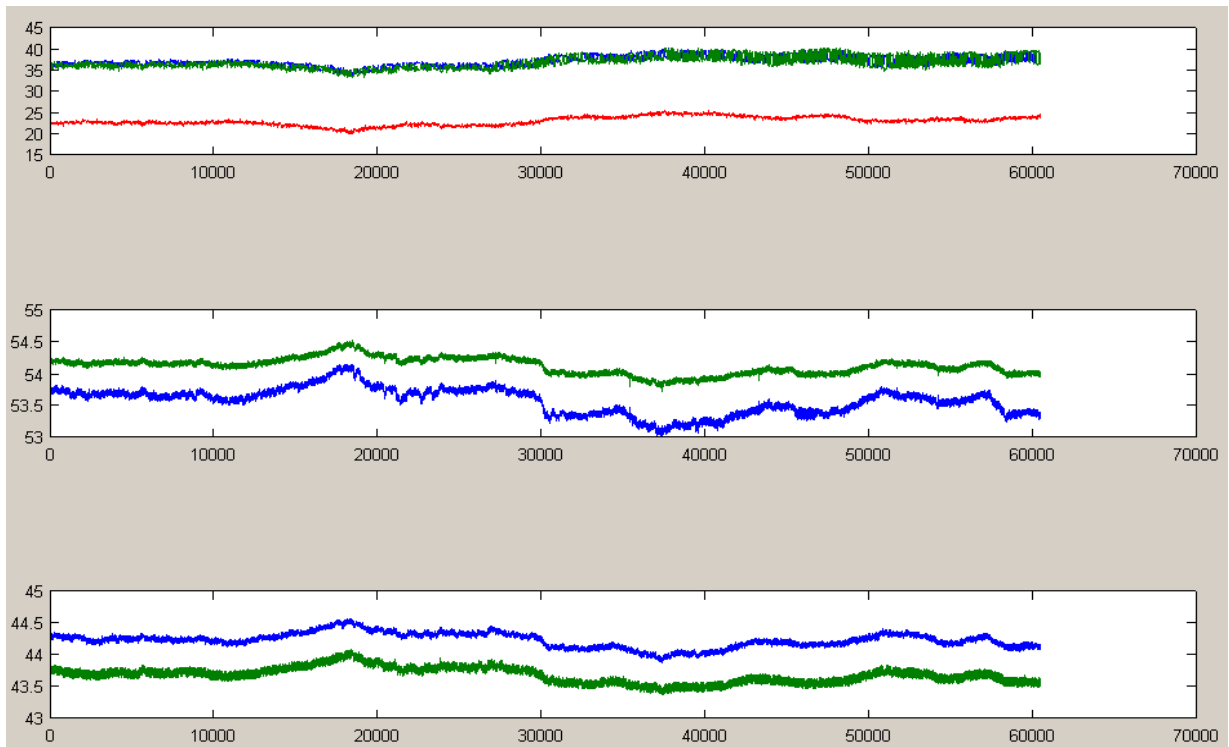


Figure 4: Data from February 27-March 6, 2009

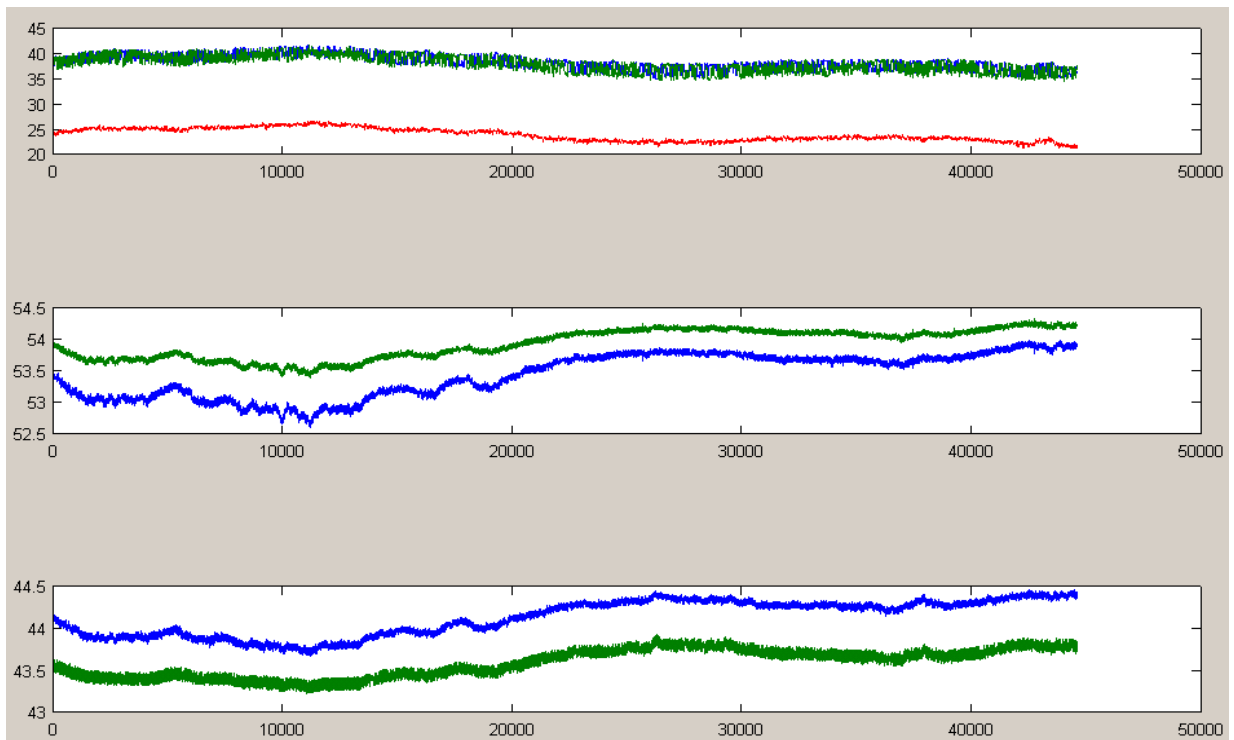


Figure 5: Data from March 6-11, 2009

The temperature plots demonstrate very clearly that the power amplifier heatsinks track the ambient air temperature with a difference of about 13 – 15 C, almost independent of the actual air temperature. This indicates that over the (+20...+30) degrees Celsius ambient temperature range encountered during the test period, the heatsink/blower system is able to dissipate the amplifier waste heat without having to rely on an increased temperature differential as the air temperature rises, i.e. it is more than large enough for ambient temperatures up to 30 °C.

RF-wise, the final amplifier stages have operated reliably for the whole 792 hours at a power level of (54 ± 0.5) dBm. An initial 0.5 dB difference in output between the two stages is maintained throughout the test period; the reason for this has not been clearly identified. There is a strong anti-correlation between ambient temperature and RF power output. While this is to be expected (all active components in the amplifier chain being majority carrier devices), most of the effect has been found to be due to gain variation with temperature in the preamplifier module. This is a two-stage device, which is operated almost 13 dB below saturation in the test bed setup. At this operating point it exhibits no gain compression to speak of, such that gain variations in both stages map linearly to the output. Figure x5 shows how the preamplifier output power varies as a function of ambient temperature over a 24-hour period. An 8-degree rise in ambient temperature causes a power gain drop of 0.8 dB. That is, in this temperature range the preamplifier module exhibits a dP/dt of -0.1 dB/°C.

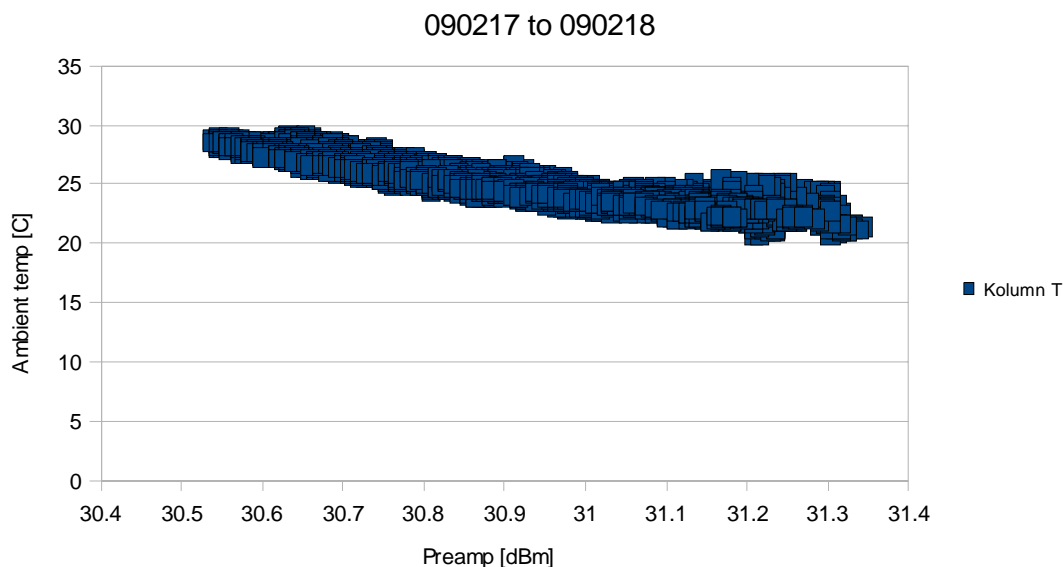


Figure 6: Graph of the gain vs. temperature variation of the Mitsubishi RA30H2127M RF power module used as pre-amplifier in the EISCAT_3D RF power test bed.

In the full 3D transmitter system, a total gain between the exciter and the antenna in the order of 60 dB will be required. Even if passive temperature compensation is employed in the low-level stages, the above observations indicate that some degree of temperature-dependent gain variation must be expected, and it is therefore recommended that the transmitter include some form of automatic gain control to maintain the time-averaged peak output power at some preset level to within narrow tolerances ($\leq 2\%$).

Power supply effects

Many of the new radar codes now under consideration by different groups employ a combination of phase and amplitude modulation (PAM) rather than the straightforward binary phase-shift keying (BPSK) used on the present EISCAT systems. Thus the EI_3D transmitter system must be designed to replicate any deliberate amplitude modulation accurately, from the exciter all the way through to the antenna.

One of the parameters that can potentially affect the amplitude linearity of the system is the drain-source voltage applied to the final amplifier transistors. A good first approximation is that in a properly designed and loaded class-AB amplifier, a small variation of the drain voltage from its nominal value by, say, x % will manifest itself as a $2x$ % variation in output power. Since the voltage feedback loop of every stabilised power supply has a finite bandwidth and thus a characteristic time constant, such that the effective drain voltage will vary with time, perhaps even on the same time scale as the typical pulse-lengths to be used by the radar. The transient response and long-term stability of the supply used to power the amplifier therefore become important factors to consider in the overall transmitter subsystem design. Passive time constants in the bias supply circuitry (e.g. RC decoupling networks) may also affect the time-domain behaviour of the drain-source voltage to a significant degree.



Figure 7: Graphs of drain-source voltage and RF envelope measured at the output of one of the final amplifiers of the EISCAT_3D RF power test bed, operated at the 300-watt level and powered from a 28-volt switch-mode power supply.

With the EI_3D amplifiers operating off switch-mode power supplies, the RF envelope exhibits a dip of some 2 % in the middle of each 2-millisecond pulse; see Figure 6. The particular power supplies used in the test bed setup apparently have a feedback time-constant in the order of a millisecond, causing the output voltage to drop by about a volt for the first millisecond of the pulse and then building back up to 28 volts as the feedback kicks in. Connecting a 10000 μF capacitor in parallel with the load simply makes the time-constant longer; the supply voltage then drops for nearly 1.5 ms before starting to come up again.

Operating the amplifiers off a system of series-connected storage batteries, a different behaviour can be observed; see Figure 7. There is now a purely exponential drop of approximately 2 volts for the first ≈ 0.5 milliseconds of the pulse, after which the voltage stabilises; at the end of the pulse the voltage returns to its initial value with the same time constant. This is interpreted as the effect of the time constant of the RC network formed by the two 2000- μF electrolytic decoupling capacitors in each amplifier and the power supply cable resistance, $\approx 0.05 \Omega$.

The observed 2-volt variation, corresponding to a 7 % relative drop in drain voltage, does indeed cause a proportional drop in RF output voltage as is evident from the RF envelopes displayed in both Figures, consistent with the theoretically estimated 14-15 % drop in output power. This is a substantial effect; in the final system, measures must be taken to eliminate it or compensate for it by pre-distortion at the exciter level.

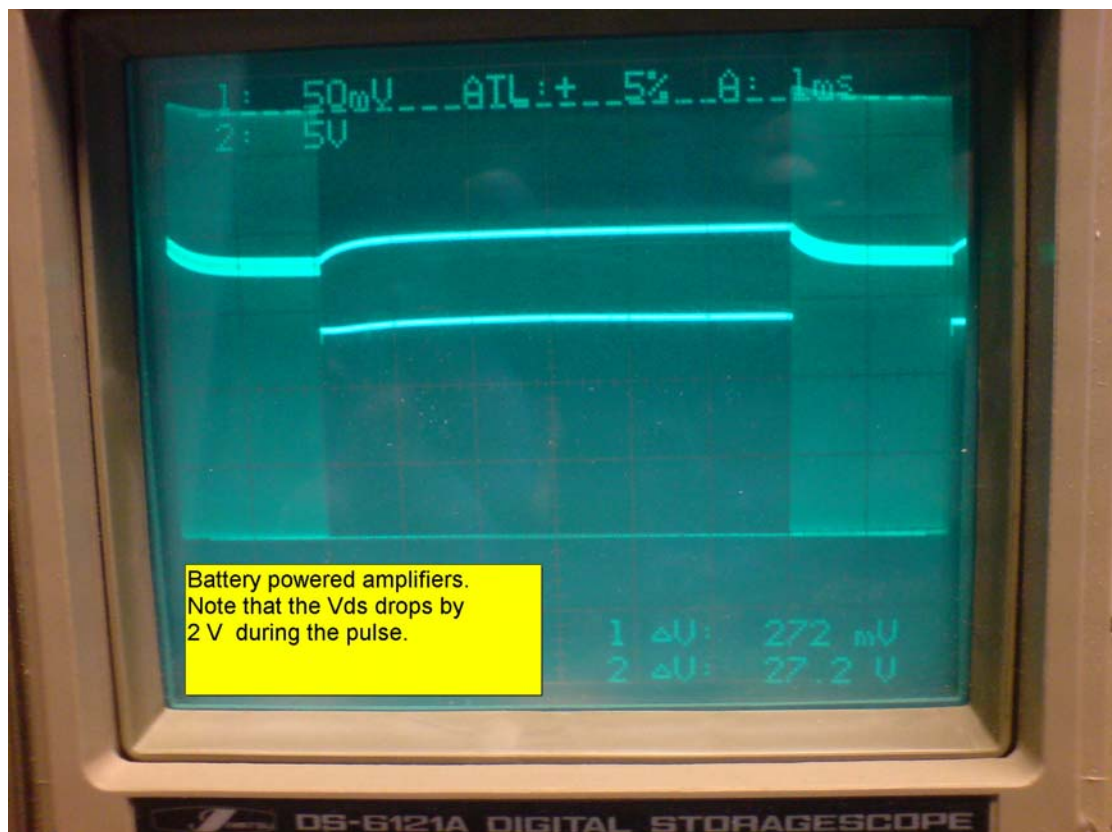


Figure 8: Graphs of drain-source voltage and RF envelope measured at the output of one of the final amplifiers of the EISCAT_3D RF power test bed, powered from a bank of series-connected storage batteries arranged to provide 28 volts.

Switching performance

Yet another factor that can potentially affect the transmitted pulse envelope is how fast the amplifiers stabilise at their normal operating points following a receive-to-transmit switchover.

The active devices used in all power amplifier stages are n-type enhancement FETs. The gate of a power FET behaves as a capacitor with an effective capacitance in the order of several hundred pF that only draws an insignificant leakage current and consumes essentially no power except when being charged or discharged. Varying the gate voltage U_G controls the drain current I_D – by taking the gate to zero volts, the electron flow from source to drain is turned off; as the gate voltage is raised to a few volts positive, I_D increases until the transistor eventually goes into saturation. FETs biased for class-AB operation are usually biased for a no-drive drain current just above the curved part of the I_D - U_G characteristic, typically 5 – 10% of the full-drive I_D .

In the test bed amplifiers, a bias switching system (schematic shown in Figure 12) maintains the gate voltages of all active devices at zero volts between RF pulses. When a pulse is about to be transmitted, the applied gate bias voltages are raised to their operating values on an external command. However, the voltages actually applied to the FET gates reach their final values only after a time determined by the bias decoupling network time constants, which in turn means that the FETs reach their final operating points after a somewhat longer delay. If RF drive is applied before all amplifier stages have settled, the output envelope during the first part of the transmission will be distorted.

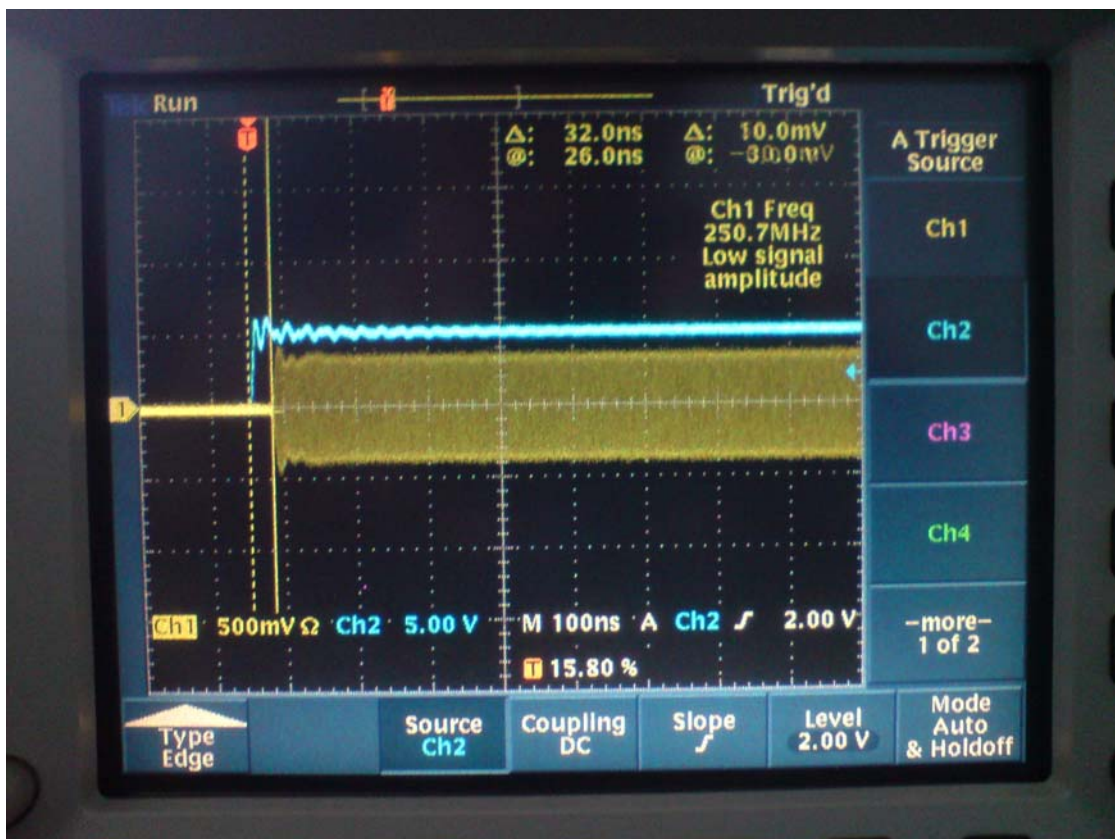


Figure 9: Preamplifier turn-on response. Full output amplitude is reached 32 ns after bias switch-on.

Accordingly, a test to investigate the amplifier turn-on behaviour has been performed. This test has been done in lieu of the high-repetition rate test mentioned in the action items listing in the Introduction, as it directly addresses the fundamental problem associated with short-pulse, high rep-rate operation. Figures 9, 10 and 11 show oscilloscope displays illustrating the output waveforms measured at the different stages of the test bed amplifier chain. In this test series, continuous-carrier low-level RF drive was applied to the preamplifier input. The bias switching system was then activated and the relationship between the logical ON command and the RF output envelope displayed on the oscilloscope.

Figure 9 shows the preamplifier output amplitude approaching its final value after 32 ns. Similarly, the driver amplifier reaches full output amplitude after 350 ns (Figure 10). The power amplifier is of course affected both by the delay of the previous stages and by the delay caused by its own time constant; it reaches full output amplitude only at 600 ns (Figure 11).

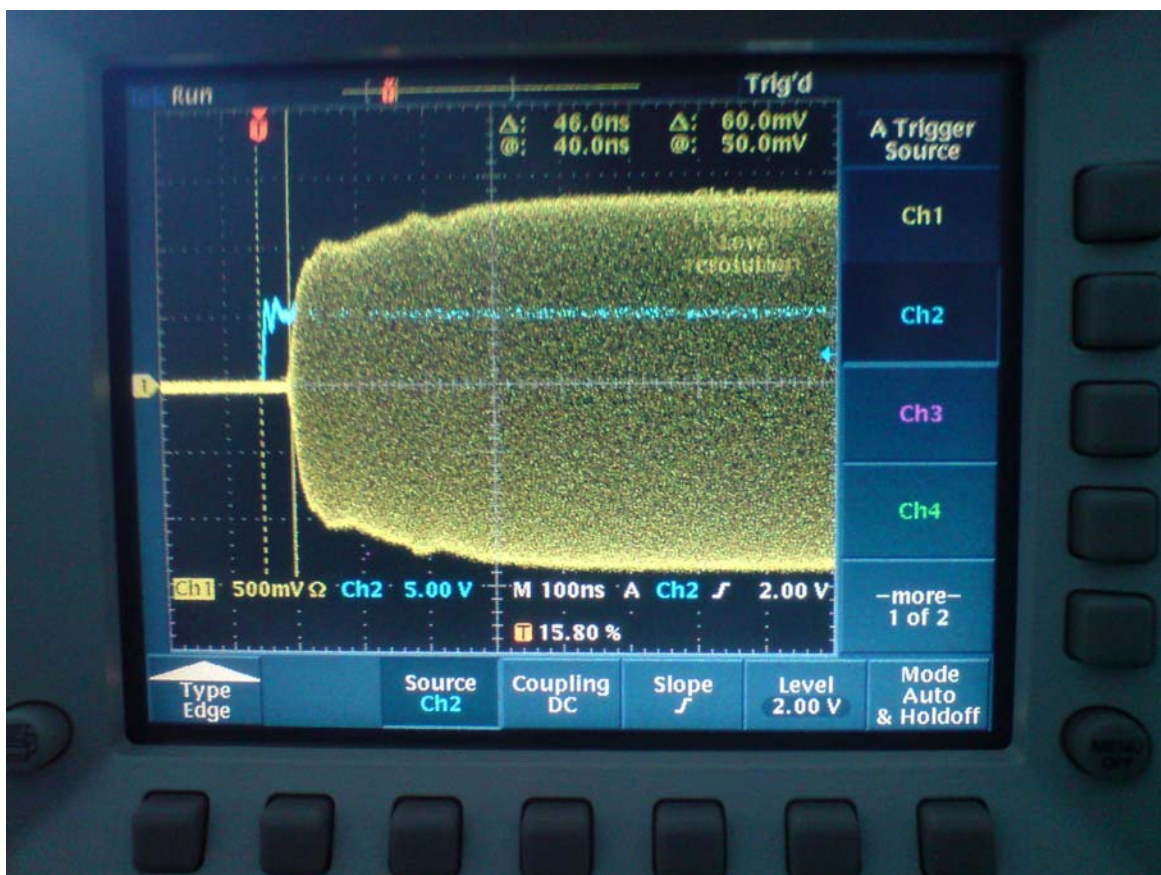


Figure 10: Driver amplifier turn-on response. Full output amplitude 350 ns after bias switch-on.

These data show that, while the amplifier chain requires a finite time to come up to full gain and output after switch-on, the waiting time required to ensure that the output pulse envelope is not badly distorted is only a couple of microseconds. The amplifier chain should therefore be fully useable also for high repetition-rate tropopause-stratosphere radar work as designed.

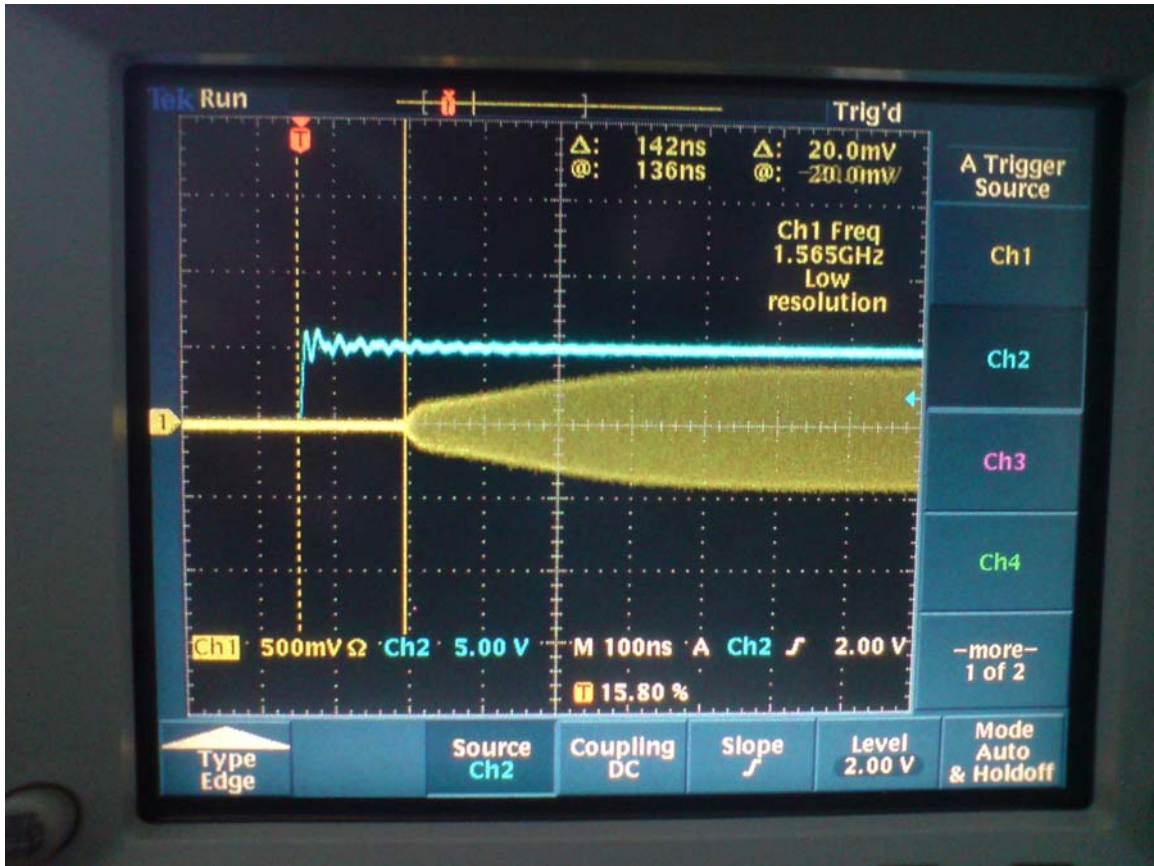


Figure 11: Final amplifier turn-on response. Full output amplitude 600 ns after bias switch-on.

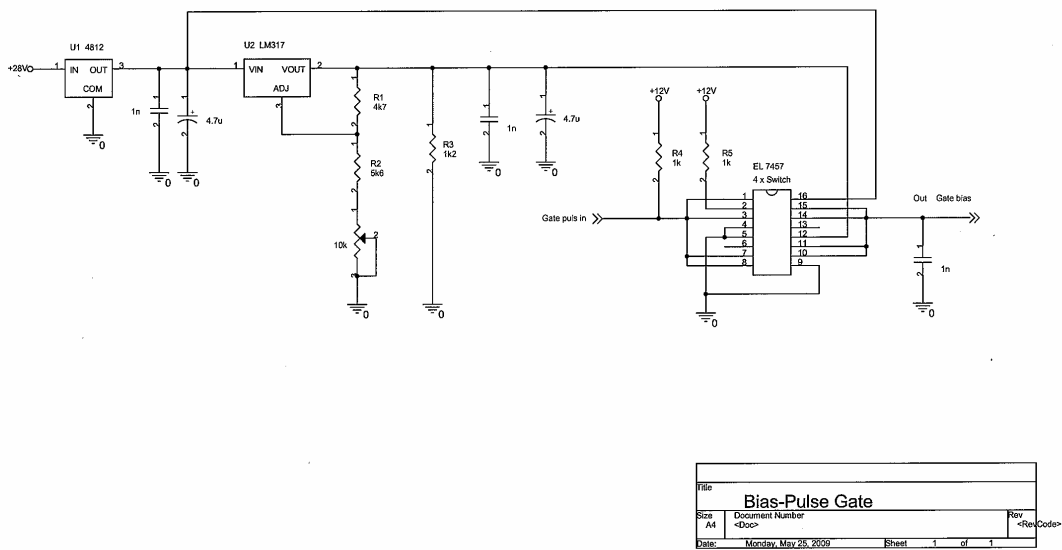


Figure 12: Circuit diagram, bias-switching system. One of these is required for each FET gate.

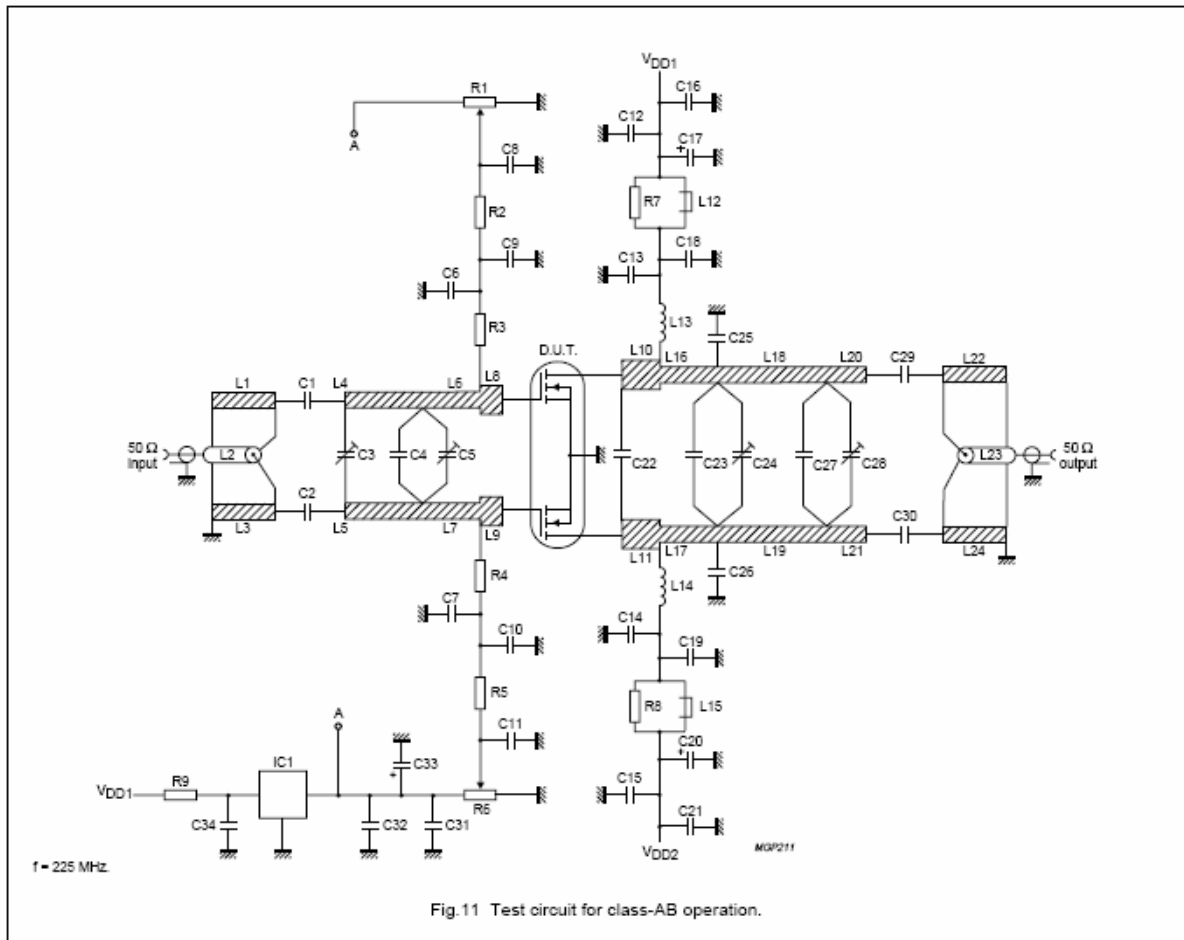


Figure 13: Schematic diagram of the BLF248 amplifier stages used as building blocks in the EISCAT_3D power test bed. Gate bias circuits have been modified according to the drawing in Figure 12 to enable gate pulsing of the device.

Saturated output power test

Following the 792-hour run, the alignment of all BLF248 amplifiers was checked and found to be close to optimum; evidently no tuning drift had taken place.

The drive level from the signal generator was then gradually raised to drive the final amplifiers almost to saturation. A brief test with continuous carrier yielded the following output power levels at -1 dB compression:

Object	Signal generator level [dBm]	Cable pad loss [dB]	Coupler test port reading [dbm]	Coupling [dB]	Output power [dBm]
Amplifier 1	8	3	19.7	-35	54.7
Amplifier 2	8	3	20.0	-35	55
Driver.	8	3	23.5	-25	48.5

The driver output is split in two branches in a hybrid splitter to provide the input signals to the two power amplifiers. The splitter loss was checked in order to calibrate the input levels to the power amplifiers. With +5 dBm going into the splitter, we measured -0.59 dBm in channel 1 and -0.68 dBm in channel 2, corresponding to an average loss of -5.6 dBm from the driver output to either power amplifier input. The drive power actually going into each final amplifier input was therefore $(48.5 - 5.6) \text{ dBm} = 42.9 \text{ dBm}$, corresponding to a final amplifier power gain of approximately 12 dB.

From April 9 to April 22, the test bed was then operated at this power setting with the same 2-ms ON, 6-ms OFF pulse scheme used for the 792-hour test with no signs of thermal fatigue or power drift. The output levels of the two final amplifiers remained at $54.7 \pm 0.5 \text{ dB}$ throughout the test period.

Phase noise measurements

Measurements made on the amplifier chain in an early phase of the test program seemed to indicate relatively poor phase noise performance. These measurements have now been repeated with much better results. Figure 14 shows the output spectrum of the overall amplifier chain running at full power with a continuous carrier, as measured through the test port at the output of final amplifier 2. The noise power density at 20 kHz offset from the carrier is now -103 dBc/Hz, which is quite good. Weak spurious sidebands can be seen at $\pm 62 \text{ kHz}$; these are assumed to be due to ripple at the PSU switching frequency (nominally 60 kHz) riding on top of the drain voltage and modulating the final amplifiers.

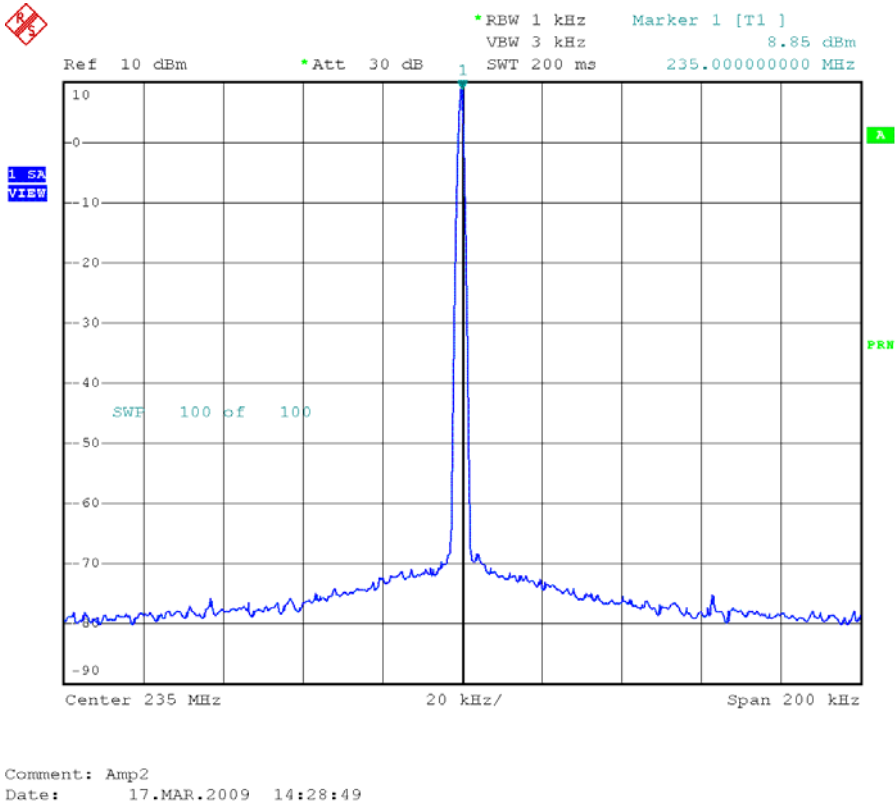


Figure 14: Power frequency spectrum of power amplifier # 2 running 300 W CW

Observations

- The BLF248 can reliably supply the required 300 watts output at 235 MHz when operated in pulsed mode with 2-millisecond full-power RF pulses every 8 milliseconds. No thermal-stress-related failures have been observed during the two extended high-power runs completed so far,
- The switch-on behaviour of the test bed power amplifier chain is such that the design could be used for the transmitter part of a high-repetition-rate, short-pulse radar for low altitude work as it stands,
- The BLF248 produces 300 watts of RF at 235 MHz only after being pushed relatively hard into compression. At that point its power gain is low, only about 12 dB.
- The power gain of the amplifier chain is strongly dependent on temperature; a 10-degree increase in ambient temperature causes the output power to drop by almost 1 dB.
- Phase noise performance is acceptable; at 20 kHz offset from the carrier the power density is better than -103 dBc /Hz.

Conclusions and recommendations

- For the full-size EISCAT_3D system, an active subsystem based on a more powerful, higher-frequency, higher-gain FET device than the BLF248 is recommended. The BLF369 may be a good choice; this device would provide at least 2 dB of dynamic headroom above the 300-watt level and would thus normally operate in an essentially linear part of its transfer function.
- To minimise temperature-dependent output variations, the low-level stages should be temperature compensated and an automatic gain control loop should be added around the whole amplifier chain.

References

- 1) EISCAT_3D Design Specification Document, http://e7.eiscat.se/groups/EISCAT_3D_info/P_S_D_7.pdf
- 2) WP 6 Interim Report, [http://e7.eiscat.se/groups/EISCAT_3D_info/D6.1 Interim Report](http://e7.eiscat.se/groups/EISCAT_3D_info/D6.1_Interim_Report)
- 3) Philips / NXP Data Sheet, BLF248 VHF push-pull power MOS transistor, http://www.nxp.com/acrobat_download/datasheets/BLF248_3.pdf

**ACTIVE ELEMENT TRANSMIT-RECEIVE
SWITCHING PERFORMANCE REQUIREMENTS**

**PIN DIODE T/R SWITCHES FOR THE ACTIVE
ELEMENT**

Gudmund Wannberg
Swedish Institute of Space Physics
Box 812
SE-98128 Kiruna, Sweden
ugw@irf.se

2008-10-29

1. Introduction

This technical note addresses the EISCAT_3D active element transmit/receive (T/R) switching subsystem. A brief overview of T/R switch basics is given, followed by a point-by-point discussion of 3D-specific T/R performance requirements (loss, isolation and noise contribution) and how a practical switch design, using readily available PIN diodes as switching elements, can be made to meet these requirements. Some comments and suggestions on how to realise the T/R subsystem in a form suitable for mass production are also offered.

2. Some T/R switch basics

Transmit-receive switches (“T/R switches”) are an important part of many radio systems where a transmitter and a co-located receiver time-share an antenna. A T/R switch is essentially a SPDT RF switch that transfers the antenna between the receiver input and the transmitter output as required. In the transmit state, it must pass the full transmitter output power to the antenna with minimal losses, while at the same time attenuating the transmitter leakage into the receiver input by as much as eight or nine orders of magnitude to protect the preamplifier from overload, degradation and possibly even burnout; in the receive state it must connect the receiver to the antenna while contributing as little extra noise as possible to the receiver noise budget. Many applications require fast switching; in e.g. short-range radar systems the switching time between transmit and receive must be less than a fraction of a microsecond!

A number of different switching technologies are employed, e.g. mechanical (coaxial relays), plasma (gas-discharge tubes and spark gaps), magnetic (ferrite circulators) and solid-state (PIN diode switches and diode limiters). With the exception of the mechanical T/R switch (which is obviously too slow), all are currently in use in different radar systems. Figure 1 shows the schematic diagram of a generic forward-current/reverse-voltage biased PIN diode T/R switch. Active-bias PIN diode T/R switches, generally similar to the Figure 1 one, have proven to be a good choice for incoherent scatter radar systems - the EISCAT VHF, UHF and ESR systems all employ such T/R switches.

The EISCAT_3D core array (1) will be constructed from thousands of individual array elements. Each element comprises a 3+3 element X-Yagi antenna, a dual transmitter power amplifier, a dual channel low-noise receiver, two T/R-switches (one for each of the two T/R-chains), timing and frequency reference subsystems and control and monitoring logic.

When in the receive state, the EISCAT_3D T/R switch must pass the received signals from the antenna to the receiver, while not adding more than 25 K to the overall system noise temperature. When in the transmit state, it must pass 350 watts of incident RF power at approximately 235 MHz to the antenna with a loss of less than -0.1 dB, or 8 watts, while at the same time isolating the receiver so thoroughly that less than -6 dBm, or 0.25 mW, RF power enters the sensitive preamplifier.

However, to make the RF system fail-safe insofar as is possible, the switch should be rated to perform even under worst-case fault conditions, e.g. when the load impedance reflected into the T/R switch antenna terminal is either a dead short or an open circuit. In the shorted case, the RF current may rise to twice its matched-load value, while in the open-circuit case the RF

voltage across the antenna terminal will be doubled. The T/R switch must survive either of these conditions indefinitely; it must also meet the receiver isolation requirement under open-circuit fault conditions. Below, we demonstrate how all the above requirements can be met by a straightforward active-bias PIN diode T/R switch design using readily available, standard components. An overview of PIN diode physics can be found in Reference 2.

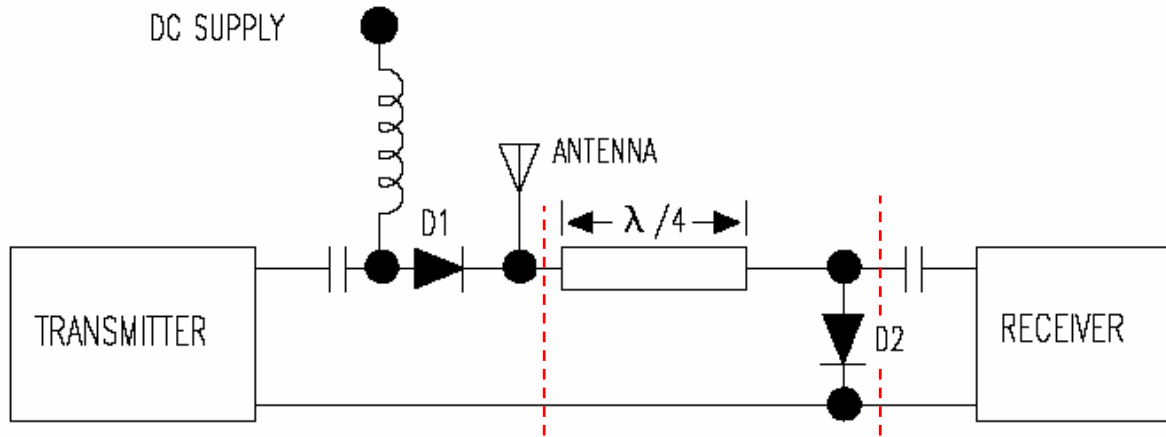


Figure 1: Schematic diagram of a series-shunt type T/R switch. D1 and D2 are PIN diodes; at each diode location several devices may be paralleled for increased power handling. Depending on the power levels involved and the PIN diode characteristics, several $\lambda/4$ -line sections (the components between the dashed red lines) may have to be inserted in series between the antenna terminal and the receiver to achieve the required TX-to-RX attenuation.

3. The EISCAT_3D core array case

3.1. TX-to-RX attenuation required for protecting the RX from degradation

Transmitter output power (nominal), P_T	350 W	= 55.4 dBm
Safety margin: multiply by 1.5, P_{TS}	525 W	= 57.2 dBm
Worst-case: total reflection at load, RF voltage at input to RX branch = 2* matched voltage ($\leftrightarrow P_{TS} + 6$ dB)		= 63.2 dBm
Max. permissible leakage power into RX, P_{Rmax}	0.25 mW	= - 6.0 dBm

=> Required attenuation through RX branch, A_{Rtx} :

$$A_{Rtx} \leq P_{Rmax} - (P_{TS} + 6 \text{ dB})$$

Numerically: $A_{Rtx} \leq - 6.0 \text{ dBm} - 63.2 \text{ dBm} = - 69.2 \text{ dB}$

In the switch topology illustrated in Figure 1, the attenuation through the $\lambda/4$ section is $A_{\lambda/4}$:

$$A_{\lambda/4} = [R_D / Z_0]^2$$

where R_D is the diode series resistance and Z_0 the $\lambda/4$ -line impedance (3). Expanding the switch to n cascaded $\lambda/4$ sections, the attenuation of each section must be

$$A_{\lambda/4} \leq (A_{Rtx})^{1/n}$$

$$\Rightarrow R_D / Z_0 = (A_{Rtx})^{1/2n} \quad \text{or} \quad \log(R_D / Z_0) = (1/20n) A_{Rtx} \text{ [dB]}$$

$$\text{Numerically } (Z_0 = 50 + j0 \Omega, A_{Rtx} = -69.2 \text{ dB}): \quad \log R_D \leq 1.70 - 3.46/n$$

To reach $A_{Rtx} = -69.2$ dB a single $\lambda/4$ section T/R would require $R_D \leq 0.017 \Omega$ - but using practical components this is totally out of reach !

However, a 2-section T/R meets the minimum A_{Rtx} requirement if $R_D \leq 1.07 \Omega$ - this is easily achieved by off-the-shelf PIN diodes, e.g. the Microsemi UM490x series: $R_D \leq 0.3 \Omega$ at 100 MHz and 100 mA bias current (4).

3.2. TX-to-ANT RF current and power handling capability

In the Figure 1 switch topology, D2 in the $\lambda/4$ -line section in the RX branch will always be exposed to the full TX output power, including possible mismatch effects. This diode, as well as the series PIN diode D1 in the TX branch, must therefore be rated to handle the full RF current and the resulting power loss.

$$\text{Transmitter output power (nominal), } P_T \quad 350 \text{ W} \quad = 55.4 \text{ dBm}$$

$$\text{Safety margin: multiply by 1.5, } P_{TS} \quad 525 \text{ W} \quad = 57.2 \text{ dBm}$$

$$\text{RMS RF current in matched } 50 \Omega \text{ load} \quad = 3.24 \text{ A}$$

$$\text{Worst-case diode current: total reflection at load,} \\ \text{RF current} = 2 * \text{matched current } (\leftrightarrow P_{TS} + 6 \text{ dB}) \quad = 6.48 \text{ A}$$

$$\text{Worst-case diode RF power loss,} \quad P_D = 4 R_D P_{TS} / Z_0$$

$$\text{If } m \text{ PIN diodes are paralleled, the power loss per diode is} \quad P_{Dm} = 4 m^{-2} R_D P_{TS} / Z_0$$

$$\text{Numerically (with above parameter values):} \quad |P_{Dm}| = 42 m^{-2} |R_D|$$

$$\text{For } m=1 \text{ and the UM490x data-sheet 100-mA bias current } R_D \text{ value, } 0.3 \Omega, P_{D1} = 12.6 \text{ W}$$

This power loss can only be handled by the stud-mounted UM490x variants (4).

For $m=2$ (two diodes in parallel) and $R_D = 0.15 \Omega$ (bias current = 300 mA) $\Rightarrow P_{D2} = 1.6 \text{ W}$
This power is easily handled by “B” (wire lead) and “E” (flat strip) style UM490x variants.
Using two UM490x diodes in parallel also in the TX series branch, the total worst-case TX power loss in the PIN diodes is $4 P_{D2} = 6.4 \text{ W}$ ($< 0.02 \text{ dB!}$)

3.3. T/R switch contribution to RX system temperature

According to 3.1, at least two $\lambda/4$ -sections will be required to ensure that $A_{R_{tx}} < -69.2$ dB. The following analysis therefore assumes the T/R switch topology illustrated in Figure 2.

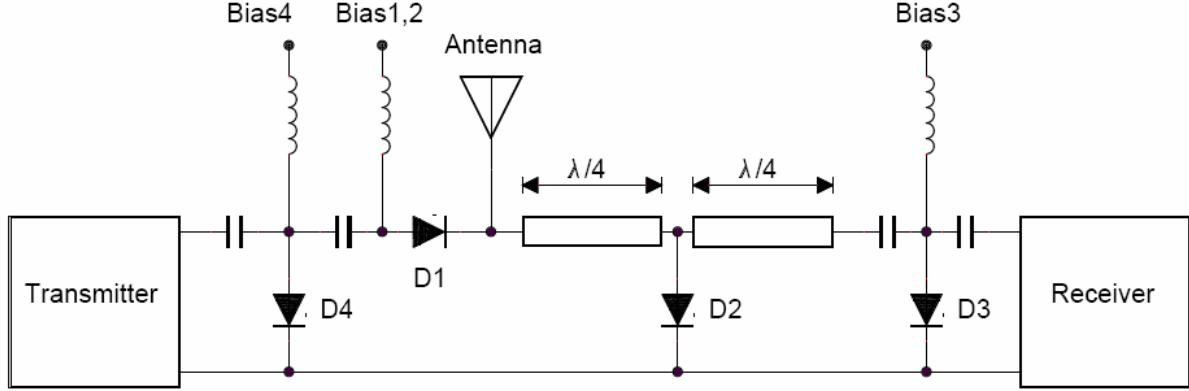


Figure 2: Schematic diagram of a dual $\lambda/4$ section series-shunt type T/R switch suitable for use in the EISCAT_3D system. Using readily available components, this switch topology can deliver better than -80 dB isolation between the antenna terminal and the RX input. D1 and D2 are identical high-power PIN diodes, rated to handle the full transmitter RF output power. D3 is a low-power, low capacitance PIN diode. D4 short-circuits the transmitter output during receive; it must be rated to withstand a reverse bias greater than the maximum peak RF voltage appearing at the antenna terminal in the transmit state.

In the EISCAT_3D system temperature budget, the contribution from the T/R switch, T_{TR} , is assumed to be ≤ 25 K. If this were entirely due to resistive losses in components at room temperature, it would correspond to a ANT-to-RX attenuation, $A_{R_{tx}} \leq -0.36$ dB. In practice, a substantial fraction of the added noise actually results from the antenna impedance being transformed by the switch, such that the preamplifier sees a source impedance $\neq 50+j0$, which moves its operating point away from the noise-optimised locus in the impedance plane. It is difficult to estimate how big this effect will be without considering the full preamplifier specifications; however, from experience it is unlikely to be bigger than the magnitude of the mismatch loss itself. In the following we therefore use the mismatch loss as a proxy for the mismatch-induced extra preamplifier noise.

3.3.1 Resistive diode loss

Assuming a diode loss resistance in the back-biased state $R_p = 30$ k Ω and a total of five PIN diodes shunted across the 50 Ω transmission line between the antenna terminal and the RX input, the equivalent shunt loss resistance R_{Loss} is

$$R_{Loss} = R_p / 5 = 6 \text{ k}\Omega$$

The power lost in this resistance is $P_{Loss} \approx (50/6000)^2$ or -42 dB of the incident power, corresponding to a through attenuation $A_{R_{Loss}}$:

$$A_{R_{Loss}} = -10 \log (1 - P_{Loss}) = -0.003 \text{ dB}$$

Impedance transformation effects have been neglected in deriving this estimate.

3.3.2 Mismatch loss

In the RX state, the diode capacitances, C_{TD1} , C_{TD2} and C_{TD3} appear as shunt reactances across the transmission line from the antenna terminal to the RX input (D4 is forward-biased in the RX state to ensure that the D1 anode is effectively at RF ground). At the antenna terminal, the receiver input impedance Z_0 now appears as a transformed impedance Z' , resulting in a mismatch loss $A_{Z'}$:

$$A_{Z'} = -10 \log (1 - (Z' / Z_0)^2)$$

A Matlab model of the Figure 2 switch topology has been used to evaluate $A_{Z'}$ for a range of D1 and D2 capacitances. The result is shown in Figure 3.

The first $\lambda/4$ section reduces the RF power incident on the second section to only a few watts. This allows the use of a low-power, low capacitance diode at D3 to reduce the impedance transformation as much as possible. In the model, D3 is assumed to be a single UM7006 (5), having a maximum P_D of only 1.5 W but a very low typical C_T of 0.8 pF at 200 V back-bias.

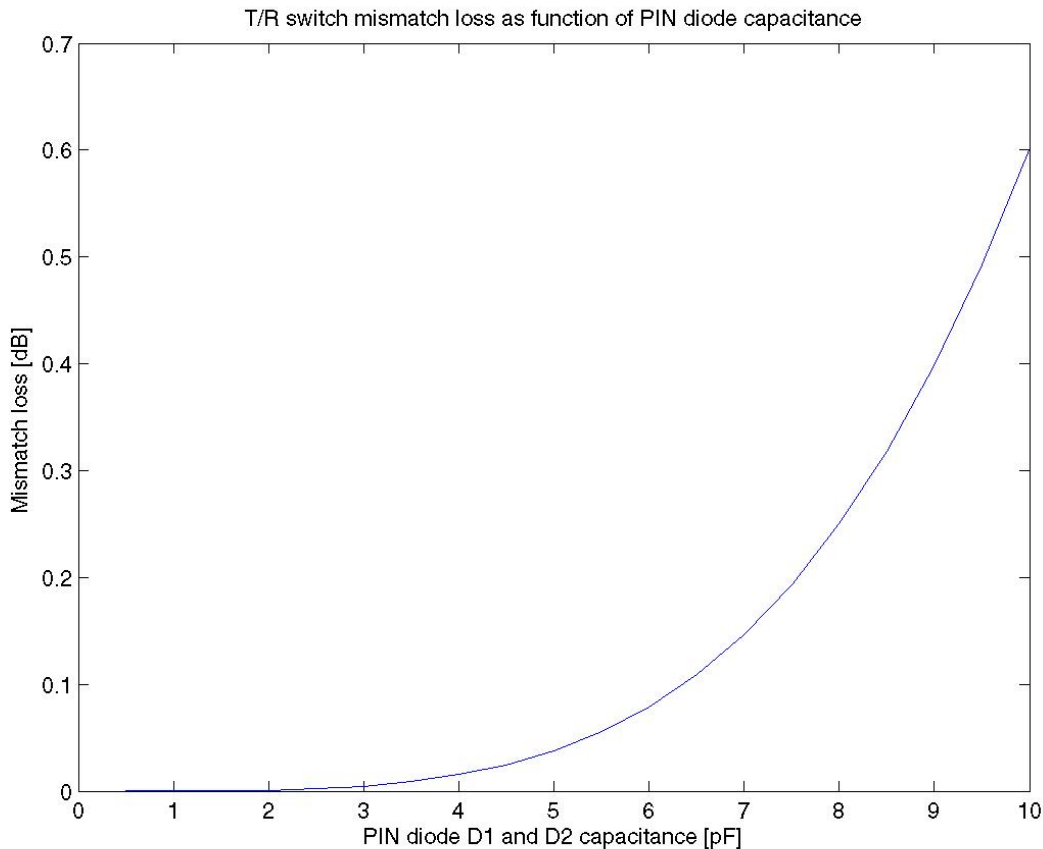


Figure 3: Mismatch loss of a dual $\lambda/4$ section series-shunt type T/R switch of the type illustrated in Figure 2, as function of the reverse-bias capacitance C_T of PIN diodes D₁ and D₂. Diode D₃ is assumed to be a UM7006.

If C_{TD1} and C_{TD2} can be kept below 8 pF each, the resulting mismatch loss is < 0.25 dB.

This can be achieved by using e.g. two paralleled UM4906 diodes at each of D₁ and D₂; these devices meet the attenuation and power-handling requirements outlined in 2.1 and 2.2 while exhibiting a C_{TD} of < 2.5 pF per diode, or < 5.0 pF for the pair.

By comparison, the resistive diode losses are negligible.

3.3.3 Other losses

Resistive losses in the $\lambda/4$ -sections and the diode bias chokes also contribute to the total.

For optimum performance, the $\lambda/4$ -sections should be realised in e.g. air-insulated stripline technology, which is intrinsically very low-loss. Since the line sections are operating with low VSWR, mismatch losses can be neglected. Each $\lambda/4$ -section can be expected to add < -0.05 dB of loss.

The discussion of mismatch losses in 3.3.2 assumes that the inductive reactances of the bias chokes supplying the high-power PIN diodes D1/D2 and D3 are essentially infinite, or at least 10-30 times greater than the capacitive reactances of their respective PIN diodes, such that they have a negligible impedance transformation effect. This can be accomplished e.g. by realising the chokes as low-loss, high-impedance ($Z > 500 \Omega$) $\lambda/4$ -section stubs, decoupled for RF at the high-current end. Losses in such stubs would be of the same order as those in the series $\lambda/4$ sections.

Alternatively, the choke inductances could have been selected to parallel-resonate the diode capacitive reactances at the design centre frequency, essentially nulling out all reactive mismatch. This technique has been used in many high-power UHF T/R switch designs, where the inductance required to resonate the system is in the order of 10-30 nH. The chokes can then be realised as short inductive stubs, shunted across the transmission line at the diode locations. However, in the present 225-240 MHz case, the required shunt inductance would be in the order of 100 nH – an unfortunate value, midway between a lumped-constant inductance and a straight stub, likely to cause mechanical design problems and therefore better avoided.

3.4 Loss budget

Mismatch loss	≤ 0.1 dB	
Losses through the $\lambda/4$ -sections	≤ 0.1 dB	
Losses in $\lambda/4$ -section bias stubs	≤ 0.1 dB	
Resistive losses (in connectors etc.)	≤ 0.05 dB	
Σ losses	≤ 0.35 dB	corresponding to $T_{TR} \leq 24.3$ K

SUMMARY:

A T/R switch of the type illustrated in Figure 2, constructed with UM4906 and UM7006 PIN diodes and low-loss $\lambda/4$ line sections and bias chokes, will meet or exceed the EISCAT_3D target specifications for:

TX-to-RX attenuation (required ≤ -69.2 dB, achieved ≤ -90 dB),

TX loss (required ≤ -0.1 dB, achieved ≤ -0.02 dB), and

RX noise-contribution (required ≤ 25 K, achieved ≤ 24.3 K)

4. Switching speed requirements

In the EISCAT_3D design specification phase, observations at altitudes below the bottom of the D layer (approx. 60 km) were not seriously considered; indeed, reference (1) does not mention observations below 80 km. However, noting that the interest of the atmosphere - ionosphere radar community is currently undergoing a shift towards lower altitudes with strong emphasis being put on processes in the neutral atmosphere, it is prudent to plan the 3D hardware for reliable operation at least from the mid-stratosphere (i.e. some 15 km) upwards. This demands overall transmit-receive switching times in the order of a few tens of microseconds at most. Whether this can be achieved in practice is a function of several parameters:

transmitter pulse length	t_T ,	
T/R switching time	t_{TRS} ,	
ringing in the antenna feed system	t_{FR}	(typically less than 1 μ s),
receiver recovery effects,	and	
ground and/or sea clutter from close-in ranges.		

In a monostatic radar system, the pulse travel time from the radar antenna to a target at range R and back is

$$t_R = 2 R/c$$

(for practical purposes, the pulse propagation speed is put $\cong c$ here; a fair approximation).

Thus $R = 15 \text{ km} \rightarrow t_R = 100 \mu\text{s}$

All of this time is not available for T/R switching, however. The system can only be switched from transmit to receive once the transmission is completed and the ringing in the feed system has died out; thus the time available for the actual T/R switching is

$$t_{TRS} \leq t_R - t_T - t_{FR}$$

Assuming that most middle atmosphere observations will employ a t_T in the order of 70 – 80 μ s in order to fully use the 3D transmitters, and that receiver recovery effects and clutter can be neglected, this gives

$$t_{TRS} \leq 15 \mu\text{s}$$

This is in the same range as the typical minority carrier lifetime τ of the UM490x series PIN diodes suggested in section 2.4 ($5 \mu\text{s} \leq \tau \leq 15 \mu\text{s}$) (4). Since, for physical reasons, $t_{TRS} \geq \tau$ (all minority carriers must recombine and/or be swept out of the diode junction before the switch-over is complete), it is clear that, even with optimised diode driver circuitry and the maximum allowed reverse bias, the lowest practical observation altitude of the 3D system will be about 15 km. This is essentially a consequence of the power handling and loss performance requirements imposed on the T/R switch, dictating the use of relatively large PIN diodes.

5. Practical realisation

Since the 3D active array will ultimately comprise upwards of 10000 elements and twice that number of T/R switch units will be required, industrial series-production philosophy must be adopted in the design and manufacturing of the T/R subsystems to be used in the actual construction, in order to facilitate their assembly and minimise mechanical and electrical complexity and production costs.

It would be extremely convenient if the T/R system could be integrated with the power amplifier and its driver amplifier into a single physical unit, according to the block diagram of Figure 4. This would bring a number of important advantages: several interconnects between the three subsystems (RF, control and monitoring) could be made internal to the unit, thus eliminating a number of cables and connectors, and the handshake and interlock functionality required to protect the unit could be combined with general control and monitoring functions in a common logic unit (possibly PIC-processor-based), so increasing the reliability, reducing the manufacturing cost and simplifying the on-site installation.

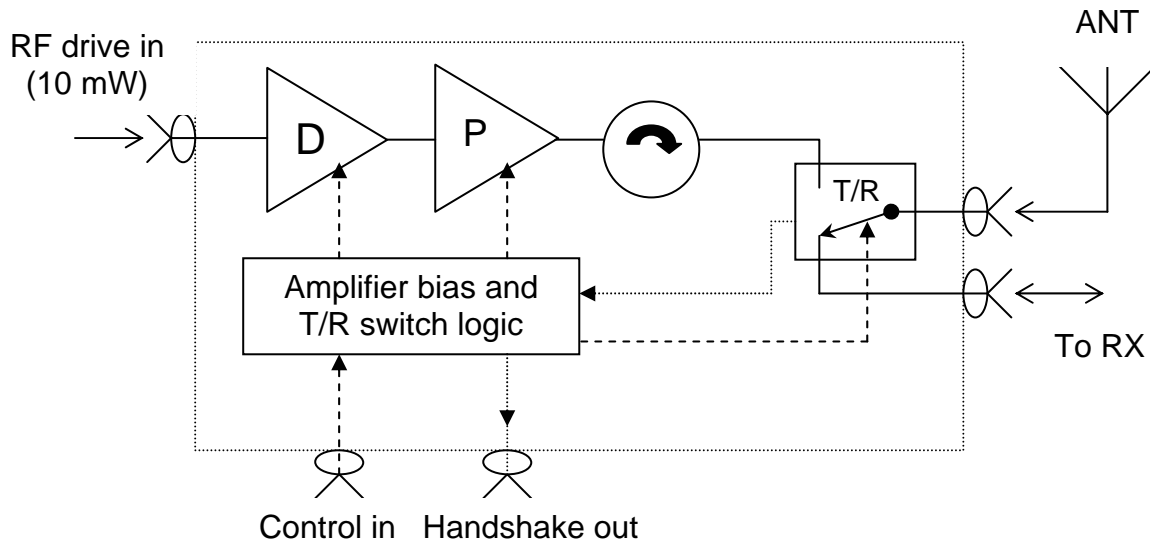


Figure 4: Block diagram of one possible realisation of the EISCAT_3D Active Element transmit, T/R switching and TX/RX control unit. Legend: D = driver amplifier (10 mW → 30 W), P = power amplifier (30 W → 350 W). Solid lines = RF signals, dashed lines = control signals, dotted lines = monitoring / handshake signals.

If printed-circuit microstripline $\lambda/4$ -sections (both 50 Ω - as well as high-impedance ones) could be shown to have sufficiently low loss and power-handling capability and still meet the system noise budget requirement, it should be possible to realise the whole driver-power amplifier-T/R switch subsystem in printed-circuit technology, thus potentially lowering the manufacturing costs dramatically as compared to a unit requiring machining to construct the line sections. To investigate whether this can be achieved in practice, some prototype units will have to be constructed and thoroughly evaluated; this is however outside the scope of the present study.

A further, but probably only marginally profitable, step towards minimising the system noise temperature would be to physically integrate also the receiver preamplifier into the T/R-power amplifier package. This would further reduce the number of interconnects and also eliminate about 10 K worth of cable-loss noise.

Irrespective of the design and construction techniques selected, bidders for the 3D construction contract should be required to demonstrate compliance with all T/R switch performance requirements through simulations and measurements performed on a small number of prototype T/R units.

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**ACTIVE ELEMENT ANTENNA ARRAY:
MUTUAL COUPLING TESTS**

Gudmund Wannberg and Ingemar Wolf
Swedish Institute of Space Physics
Box 812
SE-98128 Kiruna, Sweden
ugw@irf.se

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Mutual coupling

Mutual coupling between neighbouring elements in a phased array can ultimately limit the array performance dramatically. The radiation from one element into its neighbours sets up induced currents in these, raising the magnitude of the apparent reflection coefficient, possibly to the extent that it impairs the transmitter power amplifier performance, and causing an offset and distortion of the beam pattern in all off-boresight directions. For certain combinations of element spacings and phase offsets, a phenomenon known as *blindness* can result – all incident power is reflected and the array effectively ceases to radiate in the desired direction. The reader is referred to [3] and [4] for an in-depth treatment of these phenomena.

When designing a large phased array, it is therefore vital to verify that the degree of mutual coupling resulting from the selected combination of array geometry and radiator elements will be tolerable and that blindness will not occur anywhere within the desired field-of-view.

In the case of the EISCAT_3D Core array [1,2], this work was begun as an integral part of Mr. Renkwitz's Master's thesis work: NEC analyses of the mutual coupling and mutual impedance characteristics of the (3+3) element X "Renkwitz Yagi" were performed for a range of antenna orientations [5]. However, as the numerical results were suspiciously good and showed large variations, it was decided to validate them by actual measurement. For this purpose, a *test stand* was constructed and populated with ten Renkwitz Yagis.

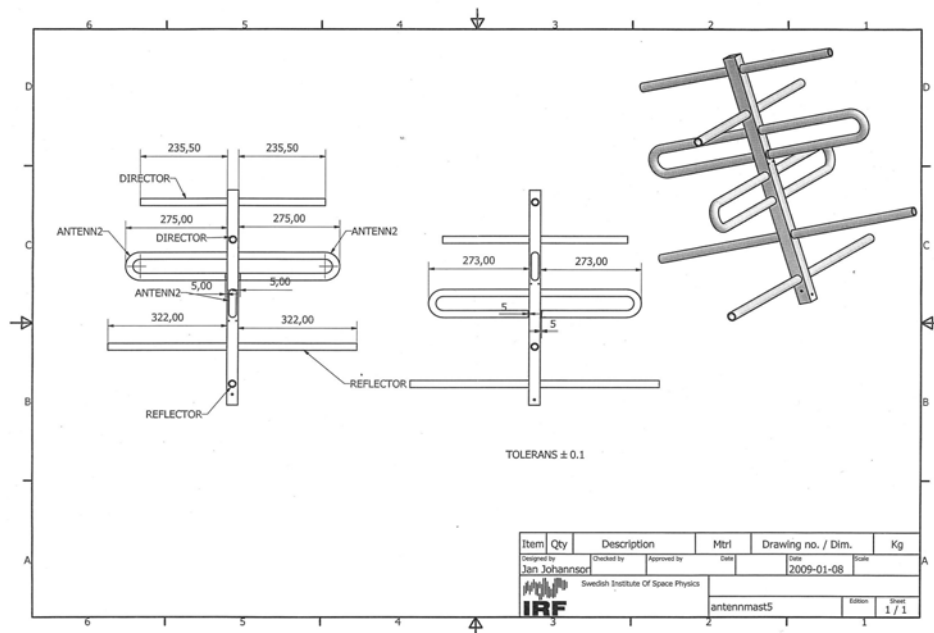


Figure 1. Mechanical drawing of the "Renkwitz Yagi" recommended for use as the element antenna in the EISCAT_3D Core array.

The Yagi antenna elements are made from 20-mm diameter aluminium tubing, welded into the boom, which is made from 30-mm square aluminium profile with 2 mm wall thickness. Two orthogonal sets of elements are mounted on the boom with a longitudinal offset of 106 mm between the sets. Half-wave baluns, made from 50-ohm RG402-type cable, transform the 200-ohm feed-point impedance of the folded dipoles to 50 ohm.



Figure 2. *Photograph of the mutual coupling test stand with ten Renkwitz Yagi antennas installed.*

The test stand is designed to replicate a sub-section of the full EI_3D core array. It can support up to nineteen antennas in an equilateral triangular geometry. It has been constructed from standard scaffolding components, supplemented by a few special details, the most important of these being the central hub, from which twelve tubular spokes radiate outwards at 30° angular separation. The hub and the outer ends of the spokes are supported on concrete blocks. The antennas under test are mounted on nineteen short lengths of aluminium tubing, one rising through the central hub and the other eighteen clamped to the spokes at variable distances from the hub, every other spoke carrying two antennas. Figure 2 shows a photograph of the test stand fully populated with all ten X Yagis in their final positions, about 1.80 m above ground.

Impedance characteristics

Before the antennas were mounted on the test stand, the complex impedance characteristics of each individual antenna were measured with a vector network analyser (VNA) to verify that all of them were operating as expected.

To speed up the measurements, the VNA was set up to operate in two-port mode; the front and rear sets of linear elements were connected to respectively the left-hand and the right-hand ports on the test set, such that the displayed s_{11} and s_{22} represented the reflection coefficients for the two polarizations. All ten antennas exceeded the predicted -20 dB $|s_{11}|$ bandwidth. As an example, Figure 3 shows the behaviour of antenna no. 8 in $|s_{xx}|$ and Smith chart format. In the upper panels, the $|s_{xx}|$ vs. frequency function predicted by the NEC simulations is overlaid in red.

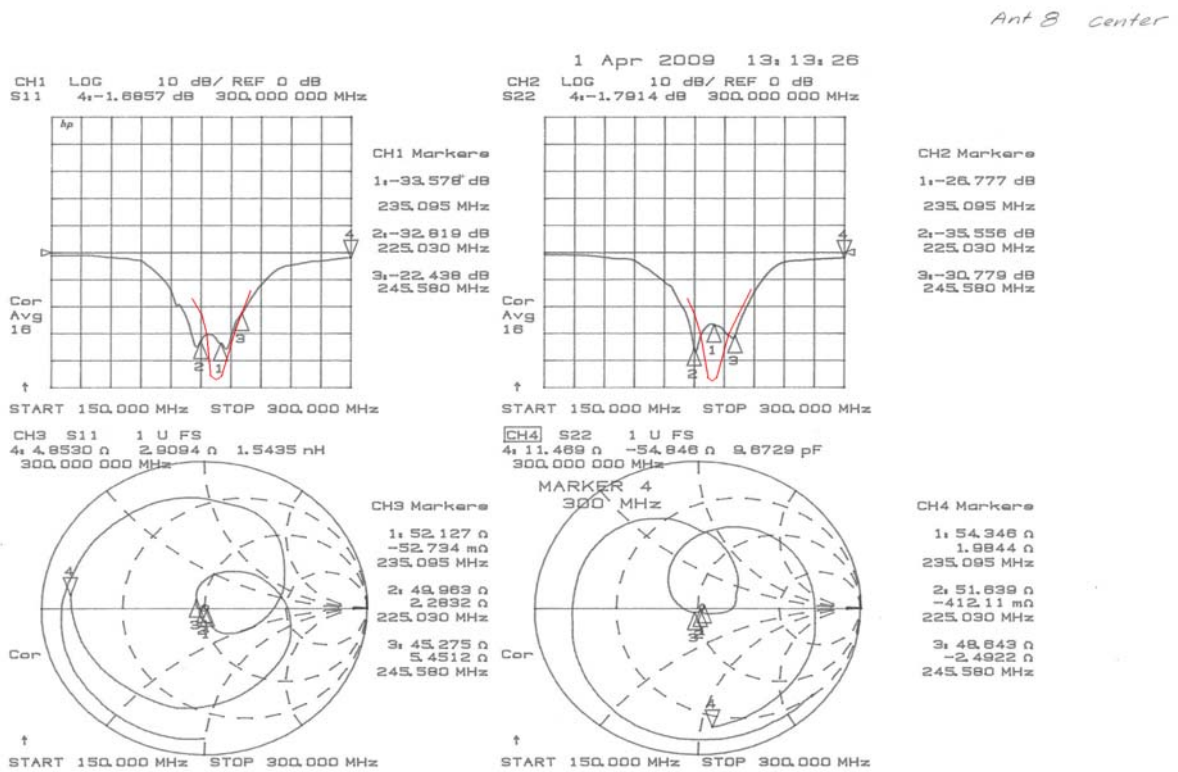


Figure 3. $|s_{xx}|$ and Smith chart plots of the feed-point impedances of the two linearly polarised systems of X Yagi no. 8.

The passbands of the physical antenna are seen to be several MHz wider than the simulated ones. Part of this effect may be due to losses in the half-wave coax cable baluns, which are not accounted for in the original NEC runs. In the next phase of the EI_3D project, this effect should be investigated further.

Mutual coupling to nearest neighbour elements

Figure 4 shows how the X Yagi antennas were installed on the test stand for the mutual coupling tests. All antenna supports were set for the 0.7λ spacing recommended in (REF) and the individual Yagi antennas were then installed with their elements oriented at 45° to the array grid line through positions E, A and F (Ren 5.3). Yagi antenna no.6 was installed in the centre position; six other antennas were grouped around it to form a closed seven-element cell and the remaining three antennas were placed in positions belonging to adjacent cells. The mutual coupling between antenna no. 6 and each of the other antennas was measured with the VNA. All antennas not connected to the VNA were terminated in $50\ \Omega$.

From the Figure, it is clear that the elements of neighbouring Yagis project onto each other to various degrees depending on their relative locations.

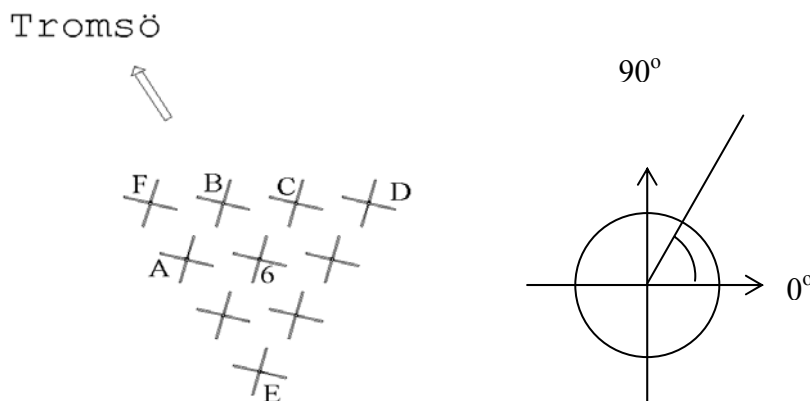


Figure 4. Schematic top view of the ten X Yagis installed on the mutual coupling test stand, showing the azimuthal orientation of their element sets. The unit circle on the right shows the 0° direction and the sense of positive rotation.

As an example, if the element system of antenna no.6 oriented in the $75^\circ - 255^\circ$ plane is excited, we can see that most of its length is projected onto the like-polarised elements in antenna A, which suggests that the mutual coupling will be strongest between these two sets of elements. A much smaller fraction is projected onto the like-polarised element set of antenna B and almost nothing onto antenna C. Due to the rotational symmetry of the array, a corresponding situation exists for the $165^\circ - 345^\circ$ polarisation but now the degree of coupling is expected to go as 6-C highest, then 6-B and 6-A. As will be seen below, the actual situation is different...

Measurements of $|s_{21}|$ were performed over the (210... 250) MHz frequency range in both linear and circular polarisation. Since so many degrees of freedom are involved, we have elected to tabulate the $|s_{21}|$ value in dB at three distinct frequencies, viz. the lower band limit, 225 MHz, mid-band, 235 MHz and the upper band limit, 245 MHz, for the respective direction A, B or C. Data for the rear and front element systems are shown separately. Mean values across the band for each direction A, B and C are also presented, as well as a mean over all directions.

In the linear polarisation measurements, only the front set of elements in antenna 6 was excited but measurements were performed both on the front and rear element sets of the other antennas; in circular polarisation, only one circularity was excited at antenna 6 but both co- and cross polarised mutual coupling were measured.

LINEAR	Centre to	225 MHz	235 MHz	245 MHz	Mean over freq. band	Mean over positions ABC
	A	-20.0	-23.7	-31.8	-23.0	
Rear	B	-25.9	-29.0	-31.0	-28.1	-25.1
	C	-24.0	-24.7	-32.5	-25.8	
	A	-21.7	-24.5	-29.4	-24.2	
Front	B	-24.8	-29.2	-35.3	-28.0	-25.5
	C	-23.3	-24.8	-29.7	-25.2	

Table 1: Mutual coupling (log magnitude) between nearest-neighbour element antennas; linear polarisation

CIRCULAR	Centre to	225 MHz	235 MHz	245 MHz	Mean over freq. band	Mean over positions ABC
	A	-34.6	-57.1	-47.5	-39.1	
Co-polar	B	-24.8	-28.5	-34.8	-27.7	-27.8
	C	-22.7	-25.0	-30.5	-25.0	
	A	-29.2	-32.2	-30.1	-30.3	
Cross-polar	B	-24.3	-27.7	-37.5	-27.3	-30.1
	C	-46.3	-52.5	-34.5	-38.9	

Table 2: Mutual coupling (log magnitude) between nearest-neighbour element antennas; circular polarisation

Mutual coupling to next-nearest neighbour elements

Measurements were also performed in linear polarisation between antenna 6 and the three next-nearest neighbour antennas installed at the extreme corners of the test array. The measured coupling values are on average 5 dB below the nearest-neighbour ones.

LINEAR	Centre to	225 MHz	235 MHz	245 MHz	Mean over freq. band	Mean over positions ABC
	D	-26.4	-26.5	-29.2	-27.2	
Front	E	-34.8	-35.0	-35.6	-35.1	-30.0
	F	-31.3	-30.9	-34.2	-31.9	

Table 3: Mutual coupling (log magnitude) between next-nearest-neighbour element antennas; linear polarisation

Discussion

The coupling between nearest-neighbour linearly polarised antennas at mid-band is on average about -25.3 dB. In circular polarisation, it is on average -29.0 dB, i.e. about 4 dB less than the linear polarisation value. However, the circular polarisation values are still almost 10 dB greater than the NEC-derived values for antennas mounted at 0.7λ above real ground; these range from a maximum of -39.9 dB to a minimum of -61.7 dB.

While a mutual coupling between nearest neighbours in the order of -29 dB is may be manageable from the transmitter point of view (it is actually of the same order as the intrinsic $|s_{11}|$ of an individual antennas at mid-band), the observed discrepancy between the NEC values and the actually measured ones is not presently well understood and sufficiently great to warrant a careful second look at the issue, including more detailed NEC runs.

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Institutet för rymdfysik

Swedish Institute of Space Physics

Swedish Institute of Space Physics
Box 812, SE- 981 28 Kiruna, SWEDEN
tel. +46-980-790 00, fax +46-980-790 50, e-post: irf@irf.se

www.irf.se